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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/633,535	08/05/2003	Yoshihiro Tsukidate	100353-00173	6456

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EXAMINER	
LE, THONG QUOC	
ART UNIT	**PAPER NUMBER**
2818	

DATE MAILED: 09/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/633,535	TSUKIDATE, YOSHIHIRO	
	Examiner	Art Unit	
	Thong Q. Le	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-10 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-8 is/are rejected.

7)☒ Claim(s) 9 and 10 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-10 are presented for examination.

Information Disclosure Statement

2. This office acknowledges receipt of the following items from the Applicant:

Information Disclosure Statement (IDS) filed on August 05, 2003.

3. Information disclosed and list on PTO 1449 was considered.

Priority

4. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Specification

5. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Title

6. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 1-8 are rejected under 35 U.S.C. 102(b) as being anticipated by Dallabora et al. (U.S. Patent No. 5,917,753).

Regarding claim 1, Dallabora et al. disclose a nonvolatile semiconductor memory device (Figure 2), comprising:

a plurality of blocks each having a memory cell array (Figure 2, 4, Column 3, lines 25-43);

a reference cell (ABSTRACT);

a signal line (Figure 2, 7, A) that supplies a reference signal read from said reference cell to each of said plurality of blocks;

a reference load circuit (ABSTRACT)which is provided in each of said plurality of blocks, and imposes a load on the reference signal that is identical to a load imposed on data that is read from said memory cell array (Column 1, lines 58-65); and

sensing circuit (Figure 1, 10) which is provided in each of said plurality of blocks, and compares the data with the reference signal having the load imposed thereon by said reference load circuit so as to sense the data (Figure 2).

Regarding claims 2-8, Dallabora et al. disclose wherein said reference load circuit includes a pass gate (Figure 1, 4) that allows the reference signal to go therethrough only in one of the blocks that is selected, and comprising a Y gate (Figure 2, 14) which is provided in each of said plurality of blocks, and selects the data read from said memory cell array, wherein a gate at last stage of said Y gate and said pass

gate are structurally identical as circuit elements, and are driven by the same potential, and comprising a gate (Figure 2, 13) that allows the reference signal to go therethrough, and corresponds to a gate other than that of the last stage of said Y gate, said gate being provided in common for each of said plurality of blocks and provided in the vicinity of said reference cell, and a boosting circuit (Figure 2, P3, P5, P4, P2) which generates a boosted potential that drives the gate at the last stage of said Y gate and said pass gate; a power supply line which supplies the boosted potential generated by said boosting circuit to each of said plurality of blocks; and switch circuit (Figure 2) which is provided in each of said plurality of blocks, and supplies the boosted potential to the gate at the last stage of said gate and said pass gate only in said one of the blocks that is selected, and and wherein said sensing circuit includes a first current-to-voltage conversion circuit (Figure 2, I/V) which converts current to voltage with respect to the data, and said reference load circuit includes second current-to-voltage conversion circuit (Figure 2, I/V) which converts current to a voltage with respect to the reference signal, wherein said first current-to-voltage conversion circuit and said second current-to-voltage conversion circuit have an identical circuit structure, and wherein said sensing circuit (Figure 1) includes first grounding circuit which couples source potential with respect to the data to a ground, and said reference load circuit includes a second grounding circuit which couples a source potential with respect to the reference signal to the ground, wherein said first grounding circuit and said second grounding circuit have an identical circuit structure, and wherein said sensing circuit further includes circuit

which short- circuits the source potential with respect to the data to the source potential with respect to the reference signal.

Allowable Subject Matter

9. Claims 9-10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 9-10 include allowable subject matter since the prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Dallabora et al. (U.S. Patent No. 5,917,753), and others, does not teach the claimed invention having the sensing circuit includes a first precharge circuit which precharges a potential of a bit line adjacent to a drain bit line with respect to the data, and said reference load circuit includes a second precharge circuit which precharges a potential of a bit line adjacent to a drain bit line with respect to the reference signal.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thong Q. Le whose telephone number is 571-272-1783. The examiner can normally be reached on 8:00am-5:00pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David C. Nelms can be reached on 571-272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thong Q. Le
Primary Examiner
Art Unit 2818

THONG LE
PRIMARY EXAMINER